ABSTRACT

A device, system and method for analysis of Very Large Scale Integration circuit designs. A computing platform may, for example, find one or more loops in a circuit design, functionally analyze the loops, and extract one or more Register-Transfer-level logical elements in relation to the analysis result. A computing platform may, for example, identify a group of at least one Channel Connected Sub-Network that forms at least one combinational loop, generate overall zero-delay collapsed functionality on an output of said group, identify one or more functional parts that form said group, and replace the group with one or more corresponding logically equivalent Register-Transfer-level devices.